ADM-XRC-6T-ADV8 User Manual

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	Head Office	US Office
Address	4 West Silvermills Lane, Edinburgh, EH3 5BD, UK	3507 Ringsby Court Suite 105 Denver, CO 80216
Telephone	+44 131 558 2600	(303) 954 8768
Fax	+44 131 558 2700	(866) 820 9956 - toll free
email	sales@alpha-data.com	sales@alpha-data.com
website	http://www.alpha-data.com	http://www.alpha-data.com

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1 Introduction

The **ADM-XRC-6T-ADV8** ("the board") is a high-performance XMC for applications using Virtex-6 FPGAs from Xilinx. This board supports those versions of the Virtex-6 LXT and SXT families available with 840 IO in the FF(G)1759 package.

The board has a single FPGA and is supplied with PCIe bridge IP developed by Alpha Data.

The board features JPEG2000 image and video capabilities using eight Analog Devices' ADV212 codecs.

The board is available in air-cooled and conduction-cooled configurations. View the ADM-XRC-6T-ADV8 specification at **ADM-XRC-6T-ADV8 Product Page** on **www.alpha-data.com**.

1.1 Key Features

Key Features

- Single-width XMC, compliant to VITA Standard 42.0 and 42.3,
- Dedicated 8-lane PCI-Express Gen 2 interface with high-performance DMA controllers,
- Support for Virtex-6 FPGA with 840 IO in FF(G)1759 package,
- 4 independent banks of DDR3-800 SDRAM, 256MB/bank, 1GB total (2GB option)
- 8 ADV212 JPEG 2000 Video CoDecs orgainised in 4 groups of 2
- Front-panel IO - 20 Rx links using two Avago "SNAP12" Optical modules @ 5.0Gb/s max per link
- Rear-panel IO (XMC)- 12 Tx and 8 Rx MGT links from P6 @ 5.0Gb/s
- Rear-panel IO (XMC)- 8 single-ended GPIO signals from P6
- Voltage and temperature monitoring

1.2 References & Specifications

AD-DS-01211	*ADM-XRC-6T-ADV8 Design Specification*, Revision 2.0, Alpha Data
ANSI/VITA 42.0	*XMC Standard*, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.3	*XMC PCI Express Protocol Layer Standard*, June 2006, VITA, ISBN 1-885731-43-4
ANSI/IEEE 1386-2001	*IEEE Standard for a Common Mezzanine Card (CMC) Family*, October 2001, IEEE, ISBN 0-7381-2829-5
ANSI/IEEE 1386.1-2001	*IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)*, October 2001, IEEE, ISBN 0-7381-2831-7

Table 1: References

2 Installation

2.1 Software Installation

Please refer to the Software Development Kit (SDK) installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

2.2 Hardware Installation

2.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe SSD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2.2 Motherboard / Carrier Requirements

The **ADM-XRC-6T-ADV8** is a single width XMC.3 mezzanine with optional P6 connector. The motherboard/ carrier must comply with the XMC.3 (VITA 42.3) specification for the Primary XMC connector, J5.

The Secondary XMC connector, J6 has a pinout compatible with VITA 46.9 "X38s + X8d + X12d" mapping. (Only 8 single-ended IO are used - see **Appendix A** for details.

> **IMPORTANT:** Connector P6 on the card is not compatible with the XMC.10 (GPIO) Standard. In particular, USB VCC must not be applied on this connector.

The supply voltage requirements for the board are shown in **Table 2** below.

Notes:

The "VPR" rail may be either 5V or 12V.

The "3.3V AUX" rail must be powered.

Voltage Level	Tolerance
3.3V	±0.3V
3.3V AUX	±0.3V
VPWR (if 5V)	±5%
VPWR (if 12V)	±5%

Table 2: XMC Voltage Requirements

The power dissipation of the board is highly dependent on the Target FPGA design. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the exact current requirements for each power rail.

2.2.3 Cooling Requirements

The power dissipation of the board is highly dependent on the user FPGA design. Although the board is supplied with a passive heatsink, the user must ensure adequate airflow over the heatsink.

The board features system monitoring that measures the board and FPGA temperature. It also includes a self-protection mechanism that will clear the target FPGA configuration if an over-temperature condition is detected.

See **Section 3.6** for further details.

3 Functional Description

3.1 Overview

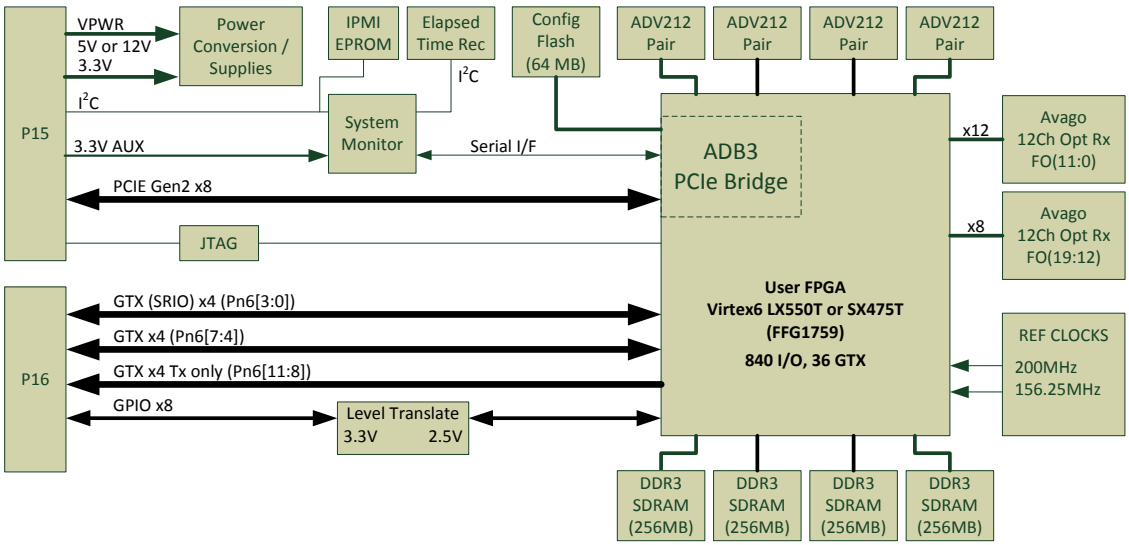

Figure 1: ADM-XRC-6T-ADV8 Block Diagram

3.1.1 Switch Definitions

There is a set of four DIP switches placed on the rear of the board. Their functions are described in **Table 3 'Switch Definitions'**.

> **Note:** All switches are OFF by default.

Switch Ref.	Function	ON State	Off State
SW1-1	XMC JTAG	Connect JTAG chain to P15	Isolate JTAG chain from P15
SW1-2	E-Fuse	Enable E-Fuse programming voltage (VccEFuse = 2.5V)	Disable E-Fuse programming voltage (VccEFuse = 0V)
SW1-3	MCU Service Mode	Enable MCU Service Mode	Disable MCU Service Mode
SW1-4	Config Sel	Select (fallback) FPGA Configuration 0	Select (default) FPGA Configuration 1

Table 3: Switch Definitions

3.1.2 LED Definitions

There are four LEDs placed on the rear of the board to indicate the status:

Comp. Ref.	Function	ON State	Off State
D7 (Amber)	MVMRO	Inhibit writes to non-volatile memories	Enable writes to non-volatile memories.
D9 (Amber)	XMC JTAG	JTAG chain connected to P15	JTAG chain is isolated from P15
D10 (Green)	SysMon0	See **Section 3.6.2**	
D11 (Red)	SysMon1	See **Section 3.6.2**	

Table 4: LED Definitions

3.2 XMC Platform Interface

3.2.1 IPMI I2C

A 2 Kbit I2C EEPROM (type M24C02) is connected to the XMC IPMI. This memory contains board information (type, voltage requirements etc.) as defined in the XMC based specification.

3.2.2 MBIST#

Built-In Self Test. This output signal is driven active (low) until the FPGA is configured.

3.2.3 MVMRO

XMC Write Prohibit. This signal is an input from the carrier. When asserted (high), all writes to non-volatile memories are inhibited. This is indicated by the Amber LED, D7.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the target FPGA at pin AC33.

3.2.4 MRSTI#

XMC Reset In. This signal is an active low input from the carrier. When asserted, the PCIe endpoint will be reset.

The MRSTI# signal is translated to 2.5V levels and connected to the target FPGA at pin AB34.

3.2.5 MRSTO#

XMC Reset Out. This optional output signal is connected to the target FPGA at pin AC34.

3.2.6 MPRESENT#

Module Present. This output signal is connected directly to 0V.

3.3 JTAG Interface

3.3.1 On-board Interface

A JTAG boundary scan chain is connected to header J1. This allows the connection of the Xilinx JTAG cable for FPGA debug using the Xilinx ChipScope tools.

The JTAG Header pinout is shown in **Figure 2, "JTAG Header J1"**:

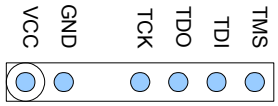

Figure 2: JTAG Header J1

The scan chain is shown in **Figure 3, "JTAG Boundary Scan Chain"**:

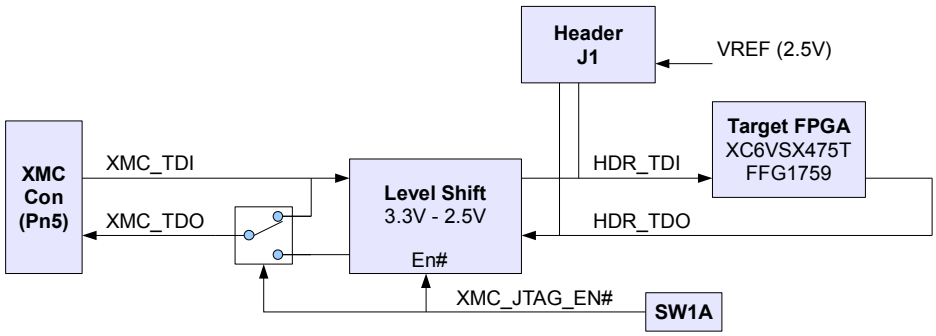

Figure 3: JTAG Boundary Scan Chain

If the boundary scan chain is connected to the interface at the XMC connector (SW1-4 is ON), Header J1 should not be used.

3.3.2 XMC Interface

The JTAG interface on the XMC connector is normally unused and XMC_TDI connected directly to XMC_TDO.

The interface can be connected to the on-board scan chain (through level-translators) by switching SW1-1 ON. See **Section 3.1.1, "Switch Definitions"**

3.3.3 JTAG Voltages

The on-board JTAG scan chain uses 2.5V. The Vcc supply provided on J1 to the JTAG cable is +2.5V and is protected by a resettable 350mA poly fuse. 3.3V signals must not be used at header J1.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

3.4 Clocks

The **ADM-XRC-6T-ADV8** has three FPGA reference clocks: the PCIe reference clock from the carrier, and two on-board references.

> **Note:** Clock Termination
> The LVDS clocks do not have termination resistors on the circuit board. On-die terminations in the FPGA must be enabled by setting the attribute "DIFF_TERM = TRUE". This can either be set in the source code when instantiating the buffer, or in the User Constraints File (UCF). See the Xilinx Virtex-6 Libraries Guide and Constraints Guide for further details.

3.4.1 PCIe Reference Clock (PCIEREFCLK)

The 100MHz PCI Express reference clock is provided by the carrier card through the Primary XMC connector, P15, at pins A19 and B19. This is connected to the target FPGA via 10nF AC coupling capacitors. On the Target FPGA, it is connected to GTX Quad 112 to allow its use as reference for the eight PCIe lanes on GTX Quads 112 and 113.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
PCIEREFCLK	MGTREFCLK0_112	LVDS_25	AK8	AK7

Table 5: PCIEREFCLK Connections

3.4.2 REFCLK200M

The fixed 200MHz reference clock, REFCLK200M, is a differential clock signal using LVDS. It is connected to a Global Clock input on the Target FPGA at pins AY14 and AY13.

This clock can be used to generate application-specific clock frequencies using the PLLs within the Virtex-6 FPGA. It is also suitable as the reference clock for the IO delay control block (IDELAYCTRL).

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK200M	IO_L0_GC_34	LVDS_25	AY14	AY13

Table 6: REFCLK200M Connections

3.4.3 MGTCLK156M

The fixed 156.25MHz reference clock, MGTCLK156M, is a differential clock signal using LVDS. The clock is buffered and connected to four MGTREFCLK inputs on the Target FPGA at GTX Quad 110, 113, 115 and 117. Since each input can clock the adjacent GTX Quads, this clock can be used by all GTX links on the board. (See Figure **Figure 6, "MGT Links"**.)

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
MGTCLK156M_A	MGTREFCLK0_117	LVDS_25	G10	G9
MGTCLK156M_B	MGTREFCLK0_115	LVDS_25	V8	V7
MGTCLK156M_C	MGTREFCLK0_113	LVDS_25	AF8	AF7
MGTCLK156M_D	MGTREFCLK0_110	LVDS_25	BA10	BA9

Table 7: MGTCLK156M Connections

3.5 Flash Memory & Configuration

A 512Mb Flash Memory (Intel / Numonyx PC28F512P30EF) is used to store configuration bitstreams for the Target FPGA.

The memory can be programmed by the host using registers in the PCIe bridge or by JTAG using Xilinx iMPACT software.

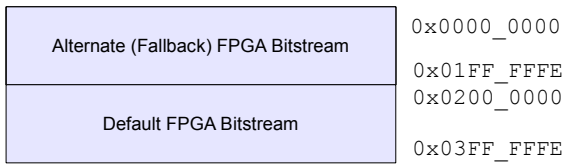

Figure 4: Flash Memory Map

3.5.1 FPGA Auto-Configuration

The memory has two sections for configuration bitstreams: a default stored at Adr 0x200_0000, and a "fallback" stored at Adr 0x000_0000.

The user bitstream should be stored in the default section. The FPGA will automatically attempt to configure with this at power-up.

The fallback section is factory programmed with a low-power design containing only the PCIe bridge and board-specific control registers. If the default bitstream is missing or corrupt, the FPGA will automatically configure with the fallback. The FPGA can be forced to configure with this bitstream by switching on SW1-4. (See Section **Section 3.1.2, "LED Definitions"**)

3.5.2 Host Programming

Using the host to program the flash is the quickest method, and utilities for erasing, programming and verification are provided in the ADMXRC SDK.

Host access is dependent on the FPGA already being configured with a design that contains the Alpha Data PCIe bridge. If this is not already in the flash memory, the FPGA can be directly configured using a JTAG programming cable. Note that the host computer will then need to be restarted for the PCIe endpoint to be useable.

3.5.3 JTAG Programming

The flash memory may be programmed over a JTAG cable using the BPI programming mode in Xilinx iMPACT software. This method does not require any host access. Programming the flash memory over JTAG is slow and best suited to stand-alone applications.

3.5.4 Flash Write Protect

The Flash Write Protect (WP#) pin is connected to an inverted version of the MVMRO signal (See Section **Section 3.2.3, "MVMRO"**) When the MVMRO signal is active (High), all writes to the flash will be inhibited. This state will be indicated by the Amber LED, D7.

3.6 System Monitoring

The **ADM-XRC-6T-ADV8** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using an Atmel AVR microcontroller (uC).

The microcontroller continually measures all voltage rails and temperature sensors and transmits the results to the FPGA, where they are stored in blockram.

The following voltage rails and temperatures are monitored by the microcontroller:

Monitor	*Purpose*
1.0V	FPGA Core Supply (VccINT)
1.5V	DDR3 SDRAM, Target FPGA memory I/O
1.8V	Flash Memory
2.5V	FPGA Auxiliary Supply (VccAUX), ADV212 I/O
CLK 2.5V	Supply for 156.25MHz clock generation
3.3V	Board Input Supply
5.0V	Internally generated 5V supply
VPWR	Board Input Supply (either 5.0V or 12.0V)
Temp1	microcontroller internal temperature
Temp2	TMP421 internal temperature
Temp3	FPGA on-die temperature (measured in TMP421)

Table 8: Voltage and Temperature Monitors (in microcontroller)

In addition, the following voltage rails and temperatures are monitored by a Xilinx System Monitor block within the FPGA:

Monitor	*Purpose*
1.0V	FPGA Core Supply (VccINT)
2.5V	FPGA Auxiliary Supply (VccAUX)
Temp4	FPGA on-die temperature (measured in FPGA)

Table 9: Voltage and Temperature Monitors (in FPGA)

The SDK includes two example applications ("sysmon" and "monitor") that read the system monitor sensor values.

3.6.1 Automatic Temperature Monitoring

The system monitor checks that the board and FPGA are being operated within the specified limits. If the temperature is close to the limit, a "Warning Alarm" interrupt is set.

If a limit is exceeded, a "Critical Alarm" interrupt is set. After the Critical Alarm is set, there is a 5 second delay before the system monitor unconfigures the FPGA by asserting its "PROG" pin.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

The temperature limits are shown in **Table 10 'Temperature Limits'**. Note that the Min and Max values include a 5°C margin to prevent measurement errors triggering a false alarm.

	Target FPGA				Board (uC and PCB)			
	Min	Lower Warning	Upper Warning	Max	Min	Lower Warning	Upper Warning	Max
Commercial	-5°C	+5°C	+80°C	+90°C	-5°C	+5°C	+65°C	+75°C
Extended	-5°C	+5°C	+95°C	+105°C	-5°C	+5°C	+80°C	+90°C
Industrial	-45°C	-35°C	+95°C	+105°C	-45°C	-35°C	+80°C	+90°C

Table 10: Temperature Limits

3.6.2 Microcontroller Status LEDs

LEDs D10 (Green) and D11 (Red) indicate the microcontroller status.

LEDs	*Status*
Flashing Green + Flashing Red (alternate)	Service Mode
Red	Missing application firmware or invalid firmware
Red + Green	Standby (Powered off)
Green	Running and no alarms
Flashing Green + Red	Attention - alarm active
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Red	FPGA configuration cleared to protect board

Table 11: Microcontroller Status

3.7 Target FPGA

3.7.1 I/O Bank Voltages

The Target FPGA IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in **Table 12 'Target FPGA IO Banks'**. Full details of the IOSTANDARD required for each signal are given in the User Constraints File within the SDK.

IO Banks	Voltage	Purpose
0, 24, 34	2.5V	Configuration, JTAG, Flash I/F, SysMon I/F
37, 38	1.5V	DRAM Bank 0
35, 36	1.5V	DRAM Bank 1
32, 33	1.5V	DRAM Bank 2
21, 22	1.5V	DRAM Bank 3
17, 25, 26, 27, 28	2.5V	ADV Pair 0 & 1
12, 13, 14, 15, 23	2.5V	ADV Pair 2 & 3
16	2.5V	Rear I/O

Table 12: Target FPGA IO Banks

3.7.2 Memory Interfaces

The board has four independent banks of DDR3 SDRAM. Each bank consists of two 16 bit wide memory devices in parallel to provide a 32 bit datapath capable of running up to 400MHz (DDR-800). 1Gb devices (Micron MT41J64M16-187E) are fitted as standard to provide 256MB per bank. 2Gb devices (giving 512MB per bank) are available as an ordering option.

The memory banks are arranged for compatibility with the Xilinx Memory Interface Generator (MIG). **Figure 5, "DRAM Banks"** Shows the component references and FPGA banks used. Full details of the interface, signaling standards and an example design are provided in the SDK.

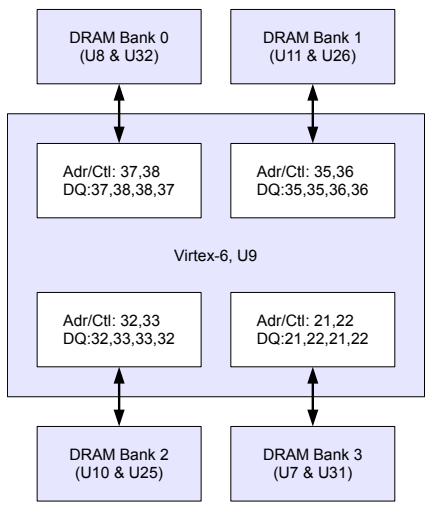

Figure 5: DRAM Banks

3.7.2.1 DCI Cascade

The DDR3 memory interfaces use the Digitally Controlled Impedance (DCI) feature within the FPGA. These require a reference voltage. To save pins on the FPGA, the reference voltage is only connected to FPGA Banks 38, 36, 32 and 21 (one per Memory interface). The other FPGA banks must use the DCI_CASCADE constraint.

For Memory Bank 0, use the constraint **CONFIG DCI_CASCADE = "38, 37"**

For Memory Bank 1, use the constraint **CONFIG DCI_CASCADE = "36, 35"**

For Memory Bank 2, use the constraint **CONFIG DCI_CASCADE = "32, 33"**

For Memory Bank 3, use the constraint **CONFIG DCI_CASCADE = "21, 22"**

3.7.3 ADV Interface

The board features 8 Analog Devices ADV212 JPEG 2000 codec devices. These devices are targeted for video and high bandwidth image compression applications. The ADV212 devices are arranged to operate independently or in four banks of two for full frame capabilities.

An example design FPGA design using the ADV212 devices is available on request.

3.7.3.1 Signal Description

Tables **Table 13 'ADV Common Signals'** and **Table 14 'ADV Individual Signals'** show the common and individual signal connections in each ADV bank.

A full pinout for the ADV Interface is supplied in the User Constraints File within the SDK.

Signal Name	Description
ADDR(3:1)	ADV212 Address Bus
MCLK	ADV212 System Clock
VCLK	ADV212 Video Data Bus Clock
HDAT(31:20, 15:0)	ADV212 Host Data Bus
JPEG_RESET_L	Asynchronous Processor Reset for ADV212s
SCOMM5	Synchronisation signal for multi-chip operation

Table 13: ADV Common Signals

Signal Name	Description
ACK_L	ADV212 Acknowledge
CS_L	ADV212 Chip Select
DACK_L(1:0)	ADV212 DMA Acknowledge
DREQ_L(1:0)	ADV212 DMA Request
IRQ_L	ADV212 Interrupt Request
RD_L	ADV212 Read Enable for Host Interface Operation
WE_L	ADV212 Write Enable for Host Interface Operation
VDAT(15:0)	ADV212 Video Data Bus
FIELD	ADV212 Field Sync for Video Mode
HSYNC	ADV212 Horizontal Sync for Video Mode
VSYNC	ADV212 Vertical Sync for Video Mode
SCOM4	ADV212 LCODE Output in Encode Mode

Table 14: ADV Individual Signals

3.7.4 Rear I/O

There are eight General Purpose I/O signals connected between the FPGA and XMC connctor P6.

The signals use 2.5V LVCMOS levels at the FPGA and 3.3V LVCMOS levels at the XMC connector. Level translation is performed by Texas Instruments TXB0108 auto-direction-sensing level translator.

Rear I/O pinout is shown in Table **Table 15 'Rear IO Pinout'** below:

Signal	FPGA Pin	XMC Pin
GP1	V33	C14
GP2	V38	F14
GP3	U34	C8
GP4	W35	F8
GP5	W38	C2
GP6	W40	F2
GP7	W37	C1
GP8	Y39	F1

Table 15: Rear IO Pinout

3.7.5 MGT Links

There are a total of 36 Multi-Gigabit Transceiver (MGT) links connected to the Target FPGA.

Links	Width	Connection
PCIe(7:0)	8	Tx\Rx PCIe connection to XMC connector P15
FrontRx(11:0)	12	Receive connection from Optical Module U13
FrontRx(19:12)	8	Receive connection from Optical Module U12
RearTx(11:0)	12	Transmit connections to XMC connector P6
RearRx(7:0)	8	Receive connections from XMC connector P6

Table 16: Target MGT Links

The connections of these links are shown in **Figure 6, "MGT Links"**:

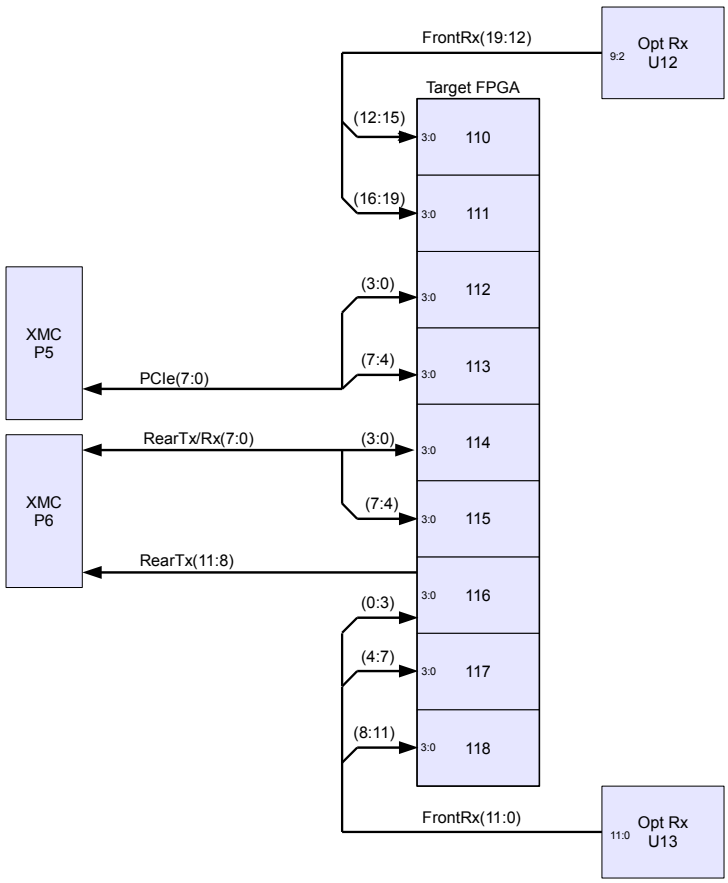

Figure 6: MGT Links

Notes:

(1) Each Quad contains a grouping of four **GTXE1** Multi-Gigabit Transceivers and two dedicated reference clock pairs.

(2) To allow optimal routing on the PCB, the links between the FPGA and optical modules are reversed. See **Table 18 'Front MGT Link Connections'** for details.

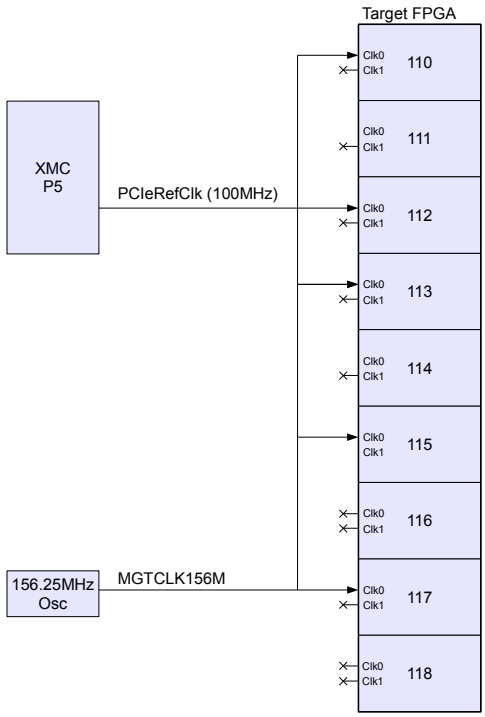

Figure 7: MGT Clocks

3.7.5.1 PCIe Links

The PCIe Links are connected to GTX Quads 112 & 113. Inside the FPGA, these should be used with the PCIe Endpoint at location PCIE_X0Y0.

The GTX locations are shown in **Table 17 'PCIe Link Connections'** below. Full pin location information is provided in a User Constraints File (UCF) within the SDK.

Signal	"P" pin	"N" pin	GTX	Location
PCIeTx(0)	AP3	AP4	112_0	GTXE1_X0Y8
PCIeTx(1)	AN1	AN2	112_1	GTXE1_X0Y9
PCIeTx(2)	AM3	AM4	112_2	GTXE1_X0Y10
PCIeTx(3)	AL1	AL2	112_3	GTXE1_X0Y11
PCIeTx(4)	AK3	AK4	113_0	GTXE1_X0Y12
PCIeTx(5)	AJ1	AJ2	113_1	GTXE1_X0Y13
PCIeTx(6)	AH3	AH4	113_2	GTXE1_X0Y14
PCIeTx(7)	AG1	AG2	113_3	GTXE1_X0Y15
PCIeRx(0)	AN5	AN6	112_0	GTXE1_X0Y8
PCIeRx(1)	AM7	AM8	112_1	GTXE1_X0Y9
PCIeRx(2)	AL5	AL6	112_2	GTXE1_X0Y10
PCIeRx(3)	AJ5	AJ6	112_3	GTXE1_X0Y11
PCIeRx(4)	AG5	AG6	113_0	GTXE1_X0Y12

Table 17: PCIe Link Connections (continued on next page)

Signal	"P" pin	"N" pin	GTX	Location
PCIeRx(5)	AF3	AF4	113_1	GTXE1_X0Y13
PCIeRx(6)	AE5	AE6	113_2	GTXE1_X0Y14
PCIeRx(7)	AD3	AD4	113_3	GTXE1_X0Y15

Table 17: PCIe Link Connections

3.7.5.2 Front MGT Links

The Front MGT Links are receive-only and are connected to Avago 12-channel optical receivers, type AFBR-785. (See Section **Section 3.8, "Optical Receiver Modules"**)

MGT links (11:0) are connected to module U13.

MGT links (19:12) are connected to channels (9:2) on module U12. Note that the central 8 channels are used to allow compatibility with both direct and crossover optical cables.

Signal	"P" pin	"N" pin	GTX	Location	Opt Module
FrontRx(0)	J5	J6	116_3	GTXE1_X0Y27	U13, lane 0
FrontRx(1)	L5	L6	116_2	GTXE1_X0Y26	U13, lane 1
FrontRx(2)	N5	N6	116_1	GTXE1_X0Y25	U13, lane 2
FrontRx(3)	P7	P8	116_0	GTXE1_X0Y24	U13, lane 3
FrontRx(4)	E5	E6	117_3	GTXE1_X0Y31	U13, lane 4
FrontRx(5)	F7	F8	117_2	GTXE1_X0Y30	U13, lane 5
FrontRx(6)	G5	G6	117_1	GTXE1_X0Y29	U13, lane 6
FrontRx(7)	H7	H8	117_0	GTXE1_X0Y28	U13, lane 7
FrontRx(8)	A5	A6	118_3	GTXE1_X0Y35	U13, lane 8
FrontRx(9)	B7	B8	118_2	GTXE1_X0Y34	U13, lane 9
FrontRx(10)	C5	C6	118_1	GTXE1_X0Y33	U13, lane 10
FrontRx(11)	D7	D8	118_0	GTXE1_X0Y32	U13, lane 11
FrontRx(12)	AW5	AW6	110_3	GTXE1_X0Y3	U12, lane 2
FrontRx(13)	AY7	AY8	110_2	GTXE1_X0Y2	U12, lane 3
FrontRx(14)	BA5	BA6	110_1	GTXE1_X0Y1	U12, lane 4
FrontRx(15)	BB7	BB8	110_0	GTXE1_X0Y0	U12, lane 5
FrontRx(16)	AP7	AP8	111_3	GTXE1_X0Y7	U12, lane 6
FrontRx(17)	AR5	AR6	111_2	GTXE1_X0Y6	U12, lane 7
FrontRx(18)	AU5	AU6	111_1	GTXE1_X0Y5	U12, lane 8
FrontRx(19)	AV7	AV8	111_0	GTXE1_X0Y4	U12, lane 9

Table 18: Front MGT Link Connections

3.7.5.3 Rear MGT Links

The rear MGT links are connected to XMC Connector P6. (See Section **Appendix A**)

RearTx(3:0) 0) are both connected to GTX Quad 114, and RearTx(7:4) 4) are connected to GTX Quad 115.

RearTx(11:8) links are connected GTX Quad 116, which is shared with FrontRx(3:0).

Signal	"P" pin	"N" pin	GTX	Location
RearTx(0)	AE1	AE2	114_0	GTXE1_X0Y16
RearTx(1)	AC1	AC2	114_1	GTXE1_X0Y17
RearTx(2)	AA1	AA2	114_2	GTXE1_X0Y18
RearTx(3)	W1	W2	114_3	GTXE1_X0Y19
RearTx(4)	U1	U2	115_0	GTXE1_X0Y20
RearTx(5)	T3	T4	115_1	GTXE1_X0Y21
RearTx(6)	R1	R2	115_2	GTXE1_X0Y22
RearTx(7)	P3	P4	115_3	GTXE1_X0Y23
RearTx(8)	N1	N2	116_0	GTXE1_X0Y24
RearTx(9)	M3	M4	116_1	GTXE1_X0Y25
RearTx(10)	L1	L2	116_2	GTXE1_X0Y26
RearTx(11)	K3	K4	116_3	GTXE1_X0Y27
RearRx(0)	AC5	AC6	114_0	GTXE1_X0Y16
RearRx(1)	AB3	AB4	114_1	GTXE1_X0Y17
RearRx(2)	AA5	AA6	114_2	GTXE1_X0Y18
RearRx(3)	Y3	Y4	114_3	GTXE1_X0Y19
RearRx(4)	W5	W6	115_0	GTXE1_X0Y20
RearRx(5)	V3	V4	115_1	GTXE1_X0Y21
RearRx(6)	U5	U6	115_2	GTXE1_X0Y22
RearRx(7)	R5	R6	115_3	GTXE1_X0Y23

Table 19: Rear MGT Link Connections

3.8 Optical Receiver Modules

3.8.1 Optical Module Reset

The two optical receiver modules share a reset input that is controlled by the FPGA. The signal OPT_RST_L is active low, connected to the FPGA at pin AU16 and uses 2.5V CMOS levels. It is connected to optical modules U12 and U13 via a 2.5V to 3.3V level translator.

A pull-up in the level translator holds the signal inactive (high) if it is not driven by the FPGA.

3.8.2 Optical Module Interrupts

Each optical receiver module has an interrupt output that is connected to the FPGA via a 3.3V to 2.5V level translator.

OPT_INT_L(0) is output from U12 and connected to the FPGA at pin AN14

OPT_INT_L(1) is output from U13 and connected to the FPGA at pin AN13

3.8.3 Optical Module I2C Interface

The optical receiver modules share an I2C interface connection to the FPGA. This allows access to the module control and status registers. These include internal voltage and temperature monitoring.

Module U12 is located at address 0101000 and module U13 at address 0101001.

Data line, OPT_SDA is connected to the FPGA at pin BA17.

Clock OPT_SCL is connected to the FPGA at pin BA16.

Both signals use 2.5V CMOS levels at the FPGA.

Appendix A: Rear Connector Pinouts

A.1: Primary XMC Connector, P5

	A	B	C	D	E	F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR(3)
2	GND	GND	XMC_TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR(3)
4	GND	GND	XMC_TCK	GND	GND	MRSTO#
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR(3)
6	GND	GND	XMC_TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR(3)
8	GND	GND	XMC_TDI	GND	GND	-12V
9	-	-	-	-	-	VPWR(5)
10	GND	GND	XMC_TDO	GND	GND	GA0
11	PER0p0	PER0n0	MBIST#	PER0p1	PER0n1	VPWR(3)
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX(2)	PER0p3	PER0n3	VPWR(3)
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	-	PER0p5	PER0n5	VPWR(3)
16	GND	GND	MVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	-	PER0p7	PER0n7	-
18	GND	GND	-	GND	GND	-
19	REFCLK+0	REFCLK-0	-	WAKE#	ROOT0#	-
Notes:	(1) PCIe Channel Lanes (7:0) are directly connected to the Target FPGA.					
	(2) 3.3V AUX is required.					
	(3) VPWR can be either +5V or +12V.					

Table A1: XMC Connector P5

A.2: Secondary XMC Connector, P6

	A	B	C	D	E	F
1	P6_TXp0	P6_TXn0	GPIO_7	P6_TXp1	P6_TXn1	GPIO_8
2	GND	GND	GPIO_5	GND	GND	GPIO_6
3	P6_TXp2	P6_TXn2	-	P6_TXp3	P6_TXn3	-
4	GND	GND	-	GND	GND	-
5	P6_TXp4	P6_TXn4	-	P6_TXp5	P6_TXn5	-
6	GND	GND	-	GND	GND	-
7	P6_TXp6	P6_TXn6	-	P6_TXp7	P6_TXn7	-
8	GND	GND	GPIO_3	GND	GND	GPIO_4
9	P6_TXp8	P6_TXn8	-	P6_TXp9	P6_TXn9	-
10	GND	GND	-	GND	GND	-
11	P6_RXp0	P6_RXn0	-	P6_RXp1	P6_RXn1	-
12	GND	GND	-	GND	GND	-
13	P6_RXp2	P6_RXn2	-	P6_RXp3	P6_RXn3	-
14	GND	GND	GPIO_1	GND	GND	GPIO_2
15	P6_RXp4	P6_RXn4	-	P6_RXp5	P6_RXn5	-
16	GND	GND	-	GND	GND	-
17	P6_RXp6	P6_RXn6	-	P6_RXp7	P6_RXn7	-
18	GND	GND	-	GND	GND	-
19	P6_TXp10	P6_TXn10	-	P6_TXp11	P6_TXn11	-
Notes:	(1) MGT Lanes are connected directly to the Target FPGA.					
	(2) GPIO signals are single-ended and 3.3V compatible.					

Table A2: XMC Connector P6

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Revision History:

Date	Revision	Nature of Change
25/07/11	0.1	First Draft
28/12/11	0.2	Second Draft., added detailed descriptions of GTX lane mappings, added microcontroller based system monitoring information, added details of optical module control interface
04/01/12	0.3	Third Draft., minor corrections
05/01/12	1.0	First issue.
31/01/12	1.1	Minor update. Added FPGA pin numbers to tables of GTX links.

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Address: 4 West Silvermills Lane,
Edinburgh, EH3 5BD, UK
Telephone: +44 131 558 2600
Fax: +44 131 558 2700
email: sales@alpha-data.com
website: http://www.alpha-data.com

Address: 3507 Ringsby Court Suite 105
Denver, CO 80216
Telephone: (303) 954 8768
Fax: (866) 820 9956 - toll free
email: sales@alpha-data.com
website: http://www.alpha-data.com